In the Claims:

1. (currently amended) A method of fabricating a MOS transistor, ~~the method~~ comprising the steps of:

creating a form structure above a starting structure, the form structure having an opening exposing a surface ~~single~~ portion of the starting structure;

forming a spacer in the opening of the form structure, the spacer extending over part of the starting structure surface and along a sidewall of the form structure opening;

~~forming~~ disposing a semiconductor material in the opening of the form structure to create a formed semiconductor body on the exposed ~~having a single generally planar bottom~~ surface of ~~above~~ the starting structure;

removing the form structure and the spacer;

forming a gate structure disposed along ~~at least a portion of a top and sides of~~ a central portion of the formed semiconductor body, the gate structure comprising a conductive gate electrode and a gate dielectric disposed between the gate electrode and the formed semiconductor body; and

doping portions of the formed semiconductor body at opposing ends of said semiconductor body to form source/drains, a portion of said semiconductor body beneath said gate structure disposed between said source/drains.

2. (currently amended)) The method of claim 1, ~~wherein the formed semiconductor body comprises a first body portion, a second body portion, and a third body portion, the second body portion being disposed between the first and third body portions and having first and second sides and a top, and~~ wherein the gate structure is formed along at least a portion of the top and sides of the central ~~second body~~ portion.

3. (currently amended) A method of fabricating a MOS transistor, the method comprising:

creating a form structure above a starting structure, the form structure having an opening exposing a single portion of the starting structure;

forming a spacer in the opening of the form structure, the spacer extending over part of the starting structure along a sidewall of the form structure opening;

forming a semiconductor material in the opening of the form structure to create a formed semiconductor body having a single generally planar bottom surface above the starting structure;

removing the form structure and the spacer;

forming a gate structure disposed along at least a portion of a top and sides of the formed semiconductor body, the gate structure comprising a conductive gate electrode and a gate dielectric disposed between the gate electrode and the formed semiconductor body; and

doping portions of the formed semiconductor body to form source/drains.

~~The method of claim 1,~~ wherein forming the spacer comprises:

depositing a first spacer material layer over the form structure and over the exposed starting structure;

depositing a second spacer material layer over the first spacer material layer; and

etching the first and second spacer material layers, leaving a portion of the first spacer material layer extending over part of the starting structure along the sidewall of the form structure opening.

4. (previously presented) The method of claim 3, wherein the spacer is generally L-shaped.

5. (previously presented) The method of claim 4, wherein depositing the first spacer material layer comprises depositing silicon nitride over the form structure and over the exposed starting structure, and wherein depositing the second spacer material layer comprises depositing silicon dioxide over the first spacer material layer.

6. (previously presented) The method of claim 5, wherein removing the form structure and the spacer comprises wet etching the form structure and the spacer, leaving the formed semiconductor body having a single generally planar bottom surface above the starting structure.

7. (previously presented) The method of claim 3, wherein removing the form structure and the spacer comprises wet etching the form structure and the spacer, leaving the formed semiconductor body having a single generally planar bottom surface above the starting structure.

8. (previously presented) The method of claim 3, wherein the first and second spacer material layers are deposited using chemical vapor deposition or atomic layer deposition.

9. (previously presented) The method of claim 1, wherein forming the spacer comprises:

depositing a spacer material layer over the form structure and over the exposed starting structure; and

etching the spacer material layer to expose a portion of the starting structure, leaving a portion of the spacer material layer extending over part of the starting structure along the sidewall of the form structure opening.

10. (previously presented) The method of claim 9, wherein depositing the spacer material layer comprises depositing silicon nitride over the form structure and over the exposed starting structure.

11. (previously presented) The method of claim 9, wherein removing the form structure and the spacer comprises wet etching the form structure and the spacer, leaving the formed semiconductor body having a single generally planar bottom surface above the starting structure.

12. (previously presented) The method of claim 9, wherein the spacer material layer is deposited using chemical vapor deposition or atomic layer deposition.

13 to 29 (canceled)